The Low-Cost and Configurable 32-Bit Soft Processor Solution

May 2005
Custom Processing On FPGA
“Have it your way”

• Xilinx Embedded Solutions
  — PicoBlaze, MicroBlaze, PowerPC 405
  — Use only the peripherals and configurations you want
  — No NRE or expensive EDA tools
  — Avoid obsolescence

• MicroBlaze - Custom Processing Made Easy
  — Pre-built, ready to use configuration options
  — Match the processor to the application
  — Platform Studio – tools customized along with the processor

• Introducing MicroBlaze v4.00
  — Floating point
  — Increased performance
  — Lower cost
MicroBlaze Processor Flexibility

• Ready to Use, Pre-Built Configuration Options

• MicroBlaze Key Features
  – 32-bit Harvard Bus RISC Architecture
    • 32 General Purpose Registers
  – Instruction and Data Caches
  – 32-bit Barrel Shifter
  – Hardware Divider
  – Fast Simplex Link FIFO Channels for Easy Direct Access to Fabric and Hardware Acceleration
    • Hardware Debug Module

• Easy-to-use Development Environment
  – Xilinx Platform Tool Suite in the Embedded Development Kit

• Third Party RTOS Support
MicroBlaze System Flexibility

1 or Multiple cores

MicroBlaze Standard 32-Bit Soft Core

Growing List of Validated and Adopted Peripherals and IP

Xilinx Virtex Family or Spartan Family of FPGAs

1 or Multiple cores

MicroBlaze Standard 32-Bit Soft Core

Growing List of Validated and Adopted Peripherals and IP

Xilinx Virtex Family or Spartan Family of FPGAs
What’s New for MicroBlaze?

• Backward compatible with MicroBlaze v3.00
• Better performance
  – Higher maximum clock frequency and fewer cycles per instruction (CPI)
• Tightly-coupled Floating-point unit (FPU)
  – IEEE754-compatible, single-precision floating point
  – FP instructions part of MicroBlaze instruction set
  – Fully supported by compiler, tools, and instruction-set simulator (ISS)
• Pattern-compare instructions for optimized comparisons
• Extending configuration flexibility
  – Configurable hardware multiplier
  – Floating point is a selectable option
• Enhanced debug logic for faster download
MicroBlaze is a soft processor core that can be implemented in the Virtex and Spartan family of FPGAs.
MicroBlaze Architecture

- **Basic Processor Functions**
- **Configurable Functions**
- **Designer Defined Blocks**
- **Peripherals – Xilinx or 3rd Party or Designer Defined**

**Components:**
- **IXCL_M** – Instruction side Xilinx Cache Link Master
- **IXCL_S** – Instruction side Xilinx Cache Link Slave
- **DXCL_M** – Data side Xilinx Cache Link Master
- **DXCL_S** – Data side Xilinx Cache Link Slave
- **MFSL** – Master Fast Simplex Link
- **SFSL** – Slave Fast Simplex Link
- **IOPB** – Instruction side On-chip Peripheral Bus
- **DOPB** – Data side On-chip Peripheral Bus
- **ILMB** – Instruction side Local Memory Bus
- **DLMB** – Data side Local Memory Bus
- **Bus Interface (Bus IF)**
- **On-chip Peripheral Bus (OPB)**
Tightly Integrated FPU

- Matched maximum clock frequency
  - FPU, MicroBlaze pipeline run at the same frequency
- Low latency
  - FP operands use native CPU registers
  - FP instructions directly integrated in data flow
- Optimum resource utilization
  - Reuse already existing pipeline resources
  - FPU adds just 1,000 LUTs to MicroBlaze

Optimized for cost and performance
# FPU Highlights

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Size (MicroBlaze + FPU)</th>
<th>Maximum Clock Frequency</th>
<th>Peak Floating-Point Throughput</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex-4</td>
<td>~2000 LUTs (1,002 FPU + 988 MB)</td>
<td>200 MHz</td>
<td>33 MFLOPS</td>
</tr>
</tbody>
</table>

## Main Hardware Configuration Options

<table>
<thead>
<tr>
<th>Feature</th>
<th>选中情况</th>
</tr>
</thead>
<tbody>
<tr>
<td>Barrel Shifter</td>
<td>○</td>
</tr>
<tr>
<td>HW Multiplier</td>
<td>○</td>
</tr>
<tr>
<td>Cache Link</td>
<td>○</td>
</tr>
<tr>
<td>Pattern Compare</td>
<td>○</td>
</tr>
<tr>
<td>HW Exception</td>
<td>○</td>
</tr>
<tr>
<td>I and D Cache</td>
<td>○</td>
</tr>
<tr>
<td>Divide</td>
<td>○</td>
</tr>
<tr>
<td>FPU</td>
<td>●</td>
</tr>
<tr>
<td>Debug Logic</td>
<td>○</td>
</tr>
</tbody>
</table>

## Frequency Optimized Subsystem

<table>
<thead>
<tr>
<th>Component</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Local Instruction Memory</td>
<td>Local Data Memory</td>
</tr>
<tr>
<td>8KB Block RAM</td>
<td>8KB Block RAM</td>
</tr>
<tr>
<td>Peripherals</td>
<td>GPIO</td>
</tr>
</tbody>
</table>
Complete FP Support

- Loads/stores use standard MicroBlaze instructions
- Infinity, signed zeros follow IEEE-754 conventions
- Software libraries for additional FPU operations
  - Rounding
  - Square root
  - Conversions
  - Other floating-point library functions

=> FPU operations seamlessly supported by standard programming model
MicroBlaze v4.00 Debug Logic

• New debug logic
  — Inserts instructions into the pipeline
  — Access to anything that instructions can access
  — Packetized data-transfer protocol

• Immediate value to users:
  — Less debug logic — reduced by 50%
  — Faster download — up to 15x faster
  — Access to all registers, including ESR, EAR, and FSR
New Pattern-Compare Instructions

• Efficient methods to compare words
  — Complement existing compare-and-branch instructions

• Example applications
  — String comparisons
  — Pattern searches
  — Multimedia applications

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>pcmpbf</td>
<td>Pattern-compare byte find</td>
</tr>
<tr>
<td>pcmpeq</td>
<td>Pattern-compare equal</td>
</tr>
<tr>
<td>pcmpeq</td>
<td>Pattern-compare not equal</td>
</tr>
</tbody>
</table>
Performance Improvements
Bringing It All Together

• Now supporting GCC 3.4.1 unit-at-a-time compile
  — Moved up from GCC 2.9 function-at-a-time compile
• New hardware and compiler boost performance
  — 0.79 DMIPS/MHz to 0.92 DMIPS/MHz
=> Overall performance benefits to users:
  — 16% performance improvement on integer code
  — Up to 40% faster string searches
  — Up to 120x performance improvement on FP code
## Configured for Performance

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Size</th>
<th>Clock Frequency</th>
<th>Dhrystone 2.1</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex-4 (4VLX25-12)</td>
<td>1,269 LUTs</td>
<td>180 MHz</td>
<td>166 DMIPS</td>
<td>0.92 DMIPS/MHz</td>
</tr>
<tr>
<td>Virtex-II Pro (2VP20-7)</td>
<td>1,225 LUTs</td>
<td>150 MHz</td>
<td>138 DMIPS</td>
<td>0.92 DMIPS/MHz</td>
</tr>
<tr>
<td>Spartan-3 (3S1500-5)</td>
<td>1,318 LUTs</td>
<td>100 MHz</td>
<td>92 DMIPS</td>
<td>0.92 DMIPS/MHz</td>
</tr>
</tbody>
</table>

### Main Hardware Configuration Options

- Barrel Shifter
- HW Multiplier
- Cache Link
- Pattern Compare
- HW Exception
- I and D Cache
- Divide
- FPU
- Debug Logic

### Performance Optimized Subsystem

<table>
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<th>Local Instruction Memory</th>
<th>Local Data Memory</th>
<th>Peripherals</th>
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<tbody>
<tr>
<td>8KB Block RAM</td>
<td>16KB Block RAM</td>
<td>GPIO, Timer</td>
</tr>
</tbody>
</table>
## Configured for Frequency

<table>
<thead>
<tr>
<th>FPGA</th>
<th>Size</th>
<th>Clock Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtex-4 (4VLX40-12)</td>
<td>988 LUTs</td>
<td>205 MHz</td>
</tr>
<tr>
<td>Virtex-II Pro (2VP20-7)</td>
<td>827 LUTs</td>
<td>170 MHz</td>
</tr>
<tr>
<td>Spartan-3 (3S1500-5)</td>
<td>983 LUTs</td>
<td>105 MHz</td>
</tr>
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</table>

### Main Hardware Configuration Options
- Barrel Shifter
- HW Multiplier
- Cache Link
- Pattern Compare
- HW Exception
- I and D Cache
- Divide
- FPU
- Debug Logic
- Frequency Optimized Subsystem
- Local Instruction Memory
- Local Data Memory
- Peripherals
- 8KB Block RAM
- 8KB Block RAM
- GPIO
MicroBlaze in Spartan-3E FPGAs
Delivering Soft Processor for Less than 50 Cents

- Customization and Flexibility
  - Rich expanding peripheral set
  - Custom peripheral support
- No Obsolescence
  - MicroBlaze source code available
- More User I/Os
- System Integration
  - Reduce cost

Effective cost as low as $0.48*

* Based on pricing for XC3S100E in 2005, 250K units
Embedded Development Kit
Accelerate Programmable System Design

• Define MicroBlaze Based Systems
  — Implement systems that interface to programmable logic
  — EDK includes MicroBlaze processor core and peripheral IP

• Complete Hardware and Software Development Environment
  — Platform Studio Technology
    • Generate custom hardware platform
    • Generate Board Support Packages “on-the-fly”
    • ‘C’ development using GNU Compiler, ‘C’ Libraries
  — Platform Debug Technology
    • Debug hardware using Xilinx Chipscope Pro bus analyzer
    • Debug software with GDB and Xilinx Debug Engine (XMD)
  — Utilize complete reference and application examples to speed development
Easy Development Tool Support

ISE Embedded Development Kit

1. VHDL or Verilog
2. HDL Entry
   - Simulation/Synthesis
   - Implementation
   - Download Bitstream Into FPGA
   - Chipscope

C Code
- Standard Embedded SW Development Flow
  - Code Entry
  - C/C++ Cross Compiler
  - Linker
  - Load Software Into FLASH
  - Debugger

Compiled ELF

Compiled BIT

RTOS, Board Support Package

Instantiate the 'System Netlist' and Implement the FPGA

HDL Entry

Download Combined Image to FPGA

Compiled ELF

Standard FPGA HW Development Flow

Easy Development Tool Support

Include the BSP and Compile the Software Image

Code Entry

C Code

VHDL or Verilog

Standard FPGA HW Development Flow

HDL Entry

Simulation/Synthesis

Implementation

Download Bitstream Into FPGA

Chipscope

Debugger
60+ Peripheral IP for MicroBlaze

Bus, Bridge and Arbiter Infrastructure
- OPB (On-chip Peripheral Bus)
- OPB PCI Arbiter
- OPB to OPB Bridge
- OPB Arbiter
- FSL Bus (Fast Simplex Link)
- LMB (Local Memory Bus)
- OPB IPIF

Memory Interface Cores
- LMB BRAM Interface Controller
- OPB External Memory Controller
- OPB SDRAM Controller
- OPB DDR SDRAM Controller
- OPB BRAM Interface Controller
- OPB System ACE Interface Controller
- Data Side BRAM Interface Controller
- Instruction Side BRAM Interface Controller

Peripherals
- OPB Interrupt Controller
- OPB 16450/16550 UART
- OPB UART Lite
- OPB IIC
- OPB SPI
- OPB PCI
- OPB Ethernet (EMAC)
- OPB Ethernet Lite (EMAC Lite)
- OPB ATMC
- OPB Single Channel HDLC
- OPB Multi Channel HDLC
- OPB Timer
- OPB Timebase WDT (Watchdog Timer)
- OPB GPIO
- OPB Central DMA Controller

...And More!
# MicroBlaze RTOS & Software Development Tools

## Xilinx Tools

<table>
<thead>
<tr>
<th>Tool</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>XMK</td>
<td>Xilinx MicroKernel</td>
</tr>
<tr>
<td></td>
<td>- Small, Modular micro kernel</td>
</tr>
<tr>
<td></td>
<td>- POSIX thread compliant, small footprint</td>
</tr>
<tr>
<td></td>
<td>- Networking, filesystem libraries</td>
</tr>
<tr>
<td>GNU</td>
<td>GNU C/C++ Compiler tools</td>
</tr>
<tr>
<td>GDB Debugger</td>
<td>GDB Debugger</td>
</tr>
<tr>
<td>XMD</td>
<td>Xilinx Microprocessor Debugger</td>
</tr>
<tr>
<td></td>
<td>- Backend Debug engine for GDB</td>
</tr>
<tr>
<td></td>
<td>- JTAG-based on-chip debug</td>
</tr>
<tr>
<td></td>
<td>- Instruction Set Simulator</td>
</tr>
<tr>
<td>lwIP</td>
<td>Light Weight IP</td>
</tr>
</tbody>
</table>

## 3rd Party Tools

- Nucleus
- ThreadX
- µC/OS-II
- µCLinux
- µITRON
- Seehau Debugger
Processor Use Models

State Machine
- Lowest Cost, No Peripherals, No RTOS & No Bus Structures
- VGA & LCD Controllers
- Low/High Performance

Microcontroller
- Medium Cost, Some Peripherals, Possible RTOS & Bus Structures
- Control & Instrumentation
- Moderate Performance

Custom Embedded
- Highest Integration, Extensive Peripherals, RTOS & Bus Structures
- Networking & Wireless
- High Performance

Range of Use Models
Case Study – Use Model 2

• Multi-Loop Industrial Control System
  – Low Cost Spartan-3

• Target Function
  – Serve as the Information Collection Hub of the System

• Requirements & Goals
  – Cost Competitive with OTS
  – Support Scalable Systems with a Wide Range of Peripherals
  – Future Proof the Solution & Show Cost Reduction over Time

<table>
<thead>
<tr>
<th></th>
<th>OTS MCU</th>
<th>μBlaze Based</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fixed solution with limited peripherals</td>
<td>Scalable to accommodate varied peripheral requirements</td>
<td></td>
</tr>
<tr>
<td>Obsolescence Concern</td>
<td>Long term product availability</td>
<td></td>
</tr>
<tr>
<td>Very few integration opportunities and difficult to customize</td>
<td>FPGA resources allow for further integration and IP customization</td>
<td></td>
</tr>
<tr>
<td>Difficult to standardize on one architecture</td>
<td>System flexibility supports a wide range of processor systems</td>
<td></td>
</tr>
</tbody>
</table>
MicroBlaze + Some IP

Completely Scalable System Architecture

66 MHz

OPB Arbiter

Inst LMB

Data LMB

MicsroBlaze

On-Chip Peripheral Bus - OPB

Internal & External Code Storage

Spartan-3

Dual Port Block RAM

UART0

UART6

Ethernet or CAN

SPI Controller

Memory Interface

完全可扩展系统架构

66 MHz

OPB仲裁器

指令LMB

数据LMB

MicroBlaze

片上外设总线 - OPB

内部及外部代码存储

Spartan-3

双向端口块RAM

UART0

UART6

以太网或CAN

SPI控制器

内存接口

完全可扩展系统架构
Xilinx Processor Solutions

1. State Machine
   - PicoBlaze™
   - MicroBlaze
   - UltraController™
   - PowerPC™

2. Microcontroller
   - MicroBlaze
   - PowerPC™
   - UltraController™

3. Custom Embedded
   - PowerPC™
   - MicroBlaze

Range of Solutions
MicroBlaze Testimonials

• “As the cost of designing and manufacturing custom chips continues to soar, processor cores optimized for FPGAs have the potential to lure designers away from ASICs and SoCs. The newest version of the Xilinx MicroBlaze processor core offers more reasons to use an FPGA, such as higher clock speeds and an optional, tightly-coupled FPU. In embedded applications such as motor control, industrial machine control, multimedia, and office automation, an FPU can make a big difference.” - Tom R. Halfhill, Sr Analyst of In-Stat's Microprocessor Report

• “The MicroBlaze processor provides a scalable solution that is fully customizable, area-efficient and can be optimized for our most cost-sensitive designs. The MicroBlaze 4.00 solution with the new FPU delivers even more performance, flexibility and ease of use, so our embedded developers can extend the life cycle of our existing products and bring new products to market even faster.”
  - Said Zahrai, Project Manager at ABB
Comprehensive Embedded Services

• **Embedded Systems Development Course (2-day course)**
  – Effectively develop, debug, and simulate an embedded system
  – Identify tools used in the EDK
  – Understand the hardware and software flows defined in the EDK
  – Understand the hardware and software simulation environments
  – Integrate custom IP into the EDK

• **On-Site Xilinx Embedded Design Specialist**
  – Provides dedicated application engineer to assist in system design, programmable logic design and embedded software development to accelerate product development
  – Deliver optimal embedded design solution for customers

• **Award-winning Technical Support**
  – Customer Hotline Support
  – MySupport.xilinx.com
  – Embedded Processor Forum and Tech Tips
Summary

• New MicroBlaze v4.00 available now
• Shipped with Xilinx Embedded Development Kit (EDK) 7.1i
• EDK 7.1i — $495 includes:
  — Platform Studio 7.1i development tools
  — Hardware and software IP support for MicroBlaze and PowerPC 405
  — MicroBlaze v4.00
• No need to be a processor expert
• No ASIC expertise required
• No NRE
• No licensing fee or royalties
• Visit www.xilinx.com/microblaze for more information

Cost, time-to-market, flexibility, and performance